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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicants: Stephen V. Kosonocky
Docket No.: YO999-369
Serial No.: 09/589,716
Filing Date: June 8, 2000
Group: 2124
Examiner: Chat C. Do

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: Lisa L. Vulpis Date: December 6, 2004

Title: Dynamic Adder with Reduced Logic

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

(1) Appeal Brief in triplicate (original and two copies); and

(2) Copy of Notice of Appeal, filed on October 1, 2004, with copy of stamped return postcard indicating receipt of Notice by PTO on October 4, 2004.

Please charge **International Business Machines Corporation Deposit Account No. 50-0510** the amount of $340 to cover this submission under 37 CFR §1.17(c). In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0510** as required to correct the error. A duplicate copy of this letter and two copies of the Appeal Brief are enclosed.

Respectfully submitted,

Robert W. Griffith

Date: December 6, 2004

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Title: Dynamic Adder with Reduced Logic

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir:

Applicant (hereinafter referred to as "Appellant") hereby appeals the final rejection of claims 1, 6-9, 11-16 and 18-20 of the above referenced application.

REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corp., as evidenced by an assignment recorded June 8, 2000 in the U.S. Patent and Trademark Office at Reel 10857, Frame 0682. The assignee, International Business Machines Corp., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

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STATUS OF CLAIMS

Claims 1-20 are pending in the present application. Claim 1 stands rejected under 35 U.S.C. §102(b), and claims 1, 6-9, 11-16 and 18-20 stand rejected under 35 U.S.C. §103(a). Claims 1, 6-9, 11-16 and 18-20 are appealed.

STATUS OF AMENDMENTS

An amendment was filed subsequent to the final rejection correcting a grammatical error in claim 8. This amendment has been entered by the Examiner.

SUMMARY OF INVENTION

The invention relates generally to logical adders and, more particularly, to a dynamic parallel adder which eliminates positive or negative complementary carry generate and propagate signal logic normally used to implement a conventional dynamic parallel adder (Specification, page 1, lines 3-6).

The present invention provides an improved implementation of a binary dynamic adder. The terms for evaluating the final sum bit are constructed from only positive (or negative) true block generate and block propagate signals, eliminating roughly half the carry logic associated with positive (or negative) complementary signal generation of the typical configuration. Expressing the final sum bit in the above form allows a simple implementation using a reduced number of dynamic logic gates (Specification, page 3, lines 2-11).

In another aspect of the invention, an *N*-bit parallel adder comprises: (i) a first logic stage, the first logic stage configured to receive a first *N*-bit binary value and a second *N*-bit binary value and compute general signals and propagate signals for each bit; (ii) a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through *m* bits from the generate and propagate signals computed in the first logic stage; (iii) a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and (iv) a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to

generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without the need for positive (or negative) complementary signal generation (Specification, page 3, line 13 through page 4, line 2).

A schematic drawing of an XOR function constructed without the need for a positive complementary version of one of its inputs, and using a combination of dynamic and static logic is illustrated in FIG. 1. Schematic drawings of dynamic logic gates used for grouping six carry signals to form a group of six carry propagate signals and six carry generate signals are illustrated in FIGS. 2 and 3, respectively. A schematic drawing of a dynamic logic gate used to perform a sum calculation using a combination of group generate and propagate signals is illustrated in FIG. 4.

By eliminating the need for positive (or negative) complementary signal generation in the parallel adder, the invention provides many benefits. For example, the invention realizes the benefits of reduced power consumption and reduced circuit area due to the elimination of positive (or negative) complementary carry logic (Specification, page 4, lines 3-6).

ISSUES PRESENTED FOR REVIEW

(I) Whether claim 1 is properly rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,905,667 to Lee (hereinafter "Lee").

(II) Whether claim 1 is properly rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 3,646,332 to Suzuki (hereinafter "Suzuki") in view of Lee.

(III) Whether claims 6-9, 11-16 and 18-20 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,943,251 to Jiang et al. (hereinafter "Jiang") in view of Lee.

GROUPING OF CLAIMS

Claims 1, 6-9, 11-16 and 18-20 do not stand or fall together. More particularly, claim 1 stands or falls alone, and claims 6-9, 11-16 and 18-20 stand or fall together.

ARGUMENT

Appellant incorporates by reference herein the disclosures of all previous responses filed in the present application, namely, responses dated June 17, 2003, October 7, 2003, April 29, 2004 and October 1, 2004. Appellant reserves the right to address the objection to the drawings in a petition, or some other action, pending the outcome of this Appeal. Sections (I), (II) and (III) to follow will respectively address issues (I), (II) and (III) presented above.

(I) With regard to the rejection of claim 1 under 35 U.S.C. §102(b) as being anticipated by Lee, Appellant asserts that Lee fails to teach or suggest each and every element respectively recited in claim 1.

It is well-established law that "[a] claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described, in a single prior art reference." See, e.g., *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). See also, M.P.E.P. §2131. Appellant asserts that the §102(e) rejection of claim 1 based on Lee fails to meet the above legal requirements for anticipation. Support for this assertion follows.

Lee discloses an adder that includes a static logic block, a first dynamic inverter logic block, a dynamic logic block, and a second dynamic inverter logic block for generating a sum through a sum output node. Lee further describes a dynamic logic version of an adder gate that uses a combination of inverting clock signals and short circuit current paths to conditionally discharge a dynamic node. This solution consumes excess power through the DC current path of the pullup device MN5 and MN71 in FIG. 5, with the pull-down trees. Lee also uses clock CLK and inverted clock CLKB to prevent a pre-discharge of the dynamic node NODE52. The outputs SUM and CARRY can be in a high-impedance floating state when CLK is low and neither the SUM or CARRY is evaluated at a HIGH signal. This creates a noise sensitivity problem.

Independent claim 1 of the present invention recites a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. FIGS. 1-3 of Lee disclose conventional adder circuits and fail to disclose an adder circuit having dynamic logic, since no clock signals are used as input. Further, FIGS. 4 and 5 of Lee both use inverted clock

signal CLKB to drive one or more dynamic nodes. In FIG. 4, inverted clock CLKB drives dynamic inversion gates 42 and 44, each of which comprises dynamic nodes. In FIG. 5, inverted clock CLKB drives dynamic node NODE52.

In response to arguments previously submitted by Appellant, the Examiner contends that FIG. 4 of Lee does not disclose any inversion signal of clock CLKB, which drives the dynamic nodes and is directly applied to the P-MOS and N-MOS transistors. More specifically, in the Advisory Action the Examiner contends that "no inverter or inverting mechanism is used in FIG. 4." However, in describing FIG. 4 in the specification of Lee (column 2, line 26 through column 3, line 43), CLK is referred to as the clock while CLKB is referred to as the inverted clock. An inverted clock signal is not simply generated separately from a clock signal. CLKB is, itself, an inverted signal of clock signal CLK. While a specific inverter is not shown in FIG. 4, it is clearly apparent from the disclosure of Lee that inverted clock signal CLKB is an inversion of clock signal CLK. Thus, since CLKB is an inversion of signal CLK which drives one or more dynamic nodes (e.g., NODE52), Appellant asserts that the circuit disclosed in Lee is distinguishable from the claimed invention.

Therefore, Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §102(b) is therefore respectfully requested.

(II) With regard to the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Lee, Appellant asserts that the Examiner has failed to set forth a proper *prima facie* case of obviousness as set forth in M.P.E.P. §2143.

Three requirements must be met to establish a *prima facie* case of obviousness. First, there must be some suggestion or motivation to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited combination must teach or suggest all the claim limitations. While it is sufficient to show that a *prima facie* case of obviousness has not been established by showing that one of the requirements has not been met, Appellant respectfully believes that none of the requirements have been met.

First, there is clear lack of motivation to combine the references. Appellant asserts that no motivation or suggestion exists to combine Suzuki and Lee in a manner proposed by the Examiner,

or to modify their teachings to meet the claim limitations. For at least this reason, a *prima facie* case of obviousness has not been established. Appellant strongly believes that one ordinarily skilled in the art would not look to Lee's dynamic logic blocks of a full adder to modify Suzuki's non-dynamic logical operation circuit device. That is, the teachings in the references are directed to completely different circuit topologies; a first (Lee) toward a dynamic adder, and a second (Suzuki) toward a non-dynamic adder. However, other than a very general and conclusory statement in the final Office Action, there is nothing in the two references that reasonably suggests why one would actually combine the teachings of these references.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Lee, 277, F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344.

In the final Office Action at page 5, the Examiner provides the following statement to prove motivation to combine Suzuki and Lee, with emphasis supplied:

> [I]t would have been obvious . . . to use the dynamic logic as disclosed in Lee's invention into Suzuki's invention because it would enable to reduce the power consumption and increase the system performance.

Appellant submits that this statement is based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. More specifically, the Examiner fails to identify any objective evidence of record which supports the proposed combination.

Second, with respect to claim 1, even assuming, *arguendo*, that the Suzuki and Lee references can be combined, Appellant asserts that there is no reasonable expectation of success in achieving the present invention through a combination of Suzuki and Lee absent the teachings of the present invention. For at least this reason, a *prima facie* case of obviousness has not been established. Despite the assertion in the final Office Action, Appellant does not believe that Suzuki and Lee are

combinable since it is not clear to one skilled in the art how one would combine the two differing circuit architectures. There is no guidance provided in the final Office Action to support such a combination. However, even if combined, they would not achieve the unique teachings of the claimed invention.

Third, Appellant asserts that even if combined, the Suzuki and Lee references, when considered either individually or in combination, fail to teach or suggest all of the limitations of claim 1. For at least this reason, a *prima facie* case of obviousness has not been established.

Independent claim 1 recites that dynamic logic is provided without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. As acknowledged by the Examiner, Suzuki does not disclose dynamic logic. Thus, while Suzuki is non-analogous art, Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic, as described above. Therefore, the combination of Suzuki and Lee also fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic.

Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §103(a) is therefore respectfully requested.

(III) With regard to the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Jiang in view of Lee, Appellant asserts that the Examiner has failed to set forth a proper *prima facie* case of obviousness as set forth in M.P.E.P. §2143.

First, there is clear lack of motivation to combine the references. Appellant asserts that no motivation or suggestion exists to combine Jiang and Lee in a manner proposed by the Examiner, or to modify their teachings to meet the claim limitations. For at least this reason, a *prima facie* case of obviousness has not been established. Appellant strongly believes that one ordinarily skilled in the art would not look to Lee's dynamic logic blocks of a full adder to modify Jiang's non-dynamic adder capable of handling multiple data of different types. That is, the teachings in the references are directed to completely different circuit topologies; one (Lee) toward a dynamic adder, the other (Jiang) toward a non-dynamic adder. However, other than a very general and conclusory statement

in the final Office Action, there is nothing in the two references that reasonably suggests why one would actually combine the teachings of these references.

In the final Office Action at page 6, the Examiner provides the following statement to prove motivation to combine Jiang and Lee, with emphasis supplied:

> [I]t would have been obvious . . . to use the dynamic logic as disclosed in Lee's invention into Jiang's invention because it would enable to reduce the power consumption and increase the system performance.

Appellant submits that this statement is based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. More specifically, the Examiner fails to identify any objective evidence of record which supports the proposed combination.

Second, with respect to claims 6-9, 11-16 and 18-20, even assuming, *arguendo*, that the Jiang and Lee references can be combined, Appellant asserts that there is no reasonable expectation of success in achieving the present invention through a combination of Jiang and Lee absent the teachings of the present invention. For at least this reason, a *prima facie* case of obviousness has not been established. Despite the assertion in the final Office Action, Appellant does not believe that Jiang and Lee are combinable since it is not clear to one skilled in the art how one would combine the two differing circuit architectures. There is no guidance provided in the final Office Action. However, even if combined, they would not achieve the unique teachings of the claimed invention.

Third, Appellant asserts that even if combined, the Jiang and Lee references, when considered either individually or in combination, fail to teach or suggest all of the limitations of claims 6-9, 11-16 and 18-20. For at least this reason, a *prima facie* case of obviousness has not been established.

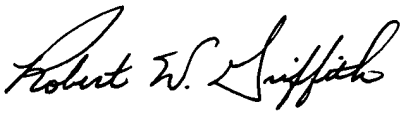
Independent claims 6, 13 and 20 recite that dynamic logic is provided without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. As acknowledged by the Examiner, Jiang does not disclose dynamic logic. Thus, while Jiang is non-analogous art, Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic, as described above. Therefore, the combination

of Jiang and Lee also fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic.

Dependent claims 7-9, 11, 12, 14-16, 18 and 19 are patentable by virtue of their dependency from independent claims 6 and 13. Dependent claims 7-9, 11, 12, 14-16, 18 and 19 also recite patentable subject matter in their own right. Accordingly, withdrawal of the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) is therefore respectfully requested.

For at least the reasons given above, Appellant respectfully requests withdrawal of the §102(b) rejection of claim 1 and the §103(a) rejections of claims 1, 6-9, 11-16 and 18-20. As such, the application is asserted to be in condition for allowance, and favorable action is respectfully solicited.

Respectfully submitted,



Date: December 6, 2004

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APPENDIX

1. Apparatus for use in summing at least two binary values, comprising:

a binary adder circuit, responsive to a first binary value, a second binary value and a carry value, and operative to generate a binary output signal S(n) representative of a summation of the first binary value, the second binary value and the carry value, the binary adder circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic, for implementing an exclusive OR function that generates the binary output value without one of a positive and a negative complementary version of the carry value.

6. A dynamic *N*-bit parallel adder, comprising:

a first logic stage, the first logic stage configured to receive a first *N*-bit binary value and a second *N*-bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through *m* bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation;

wherein at least one of the logic stages has dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic.

7. The parallel adder of claim 6, wherein a generate signal and a propagate signal computed for a bit *i* in the first logic stage represent a carry signal c_i, wherein c_i is equivalent to $g_i + (p_i\, c_{i-1})$,

where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i where a_i represents the first binary value and b_i represents the second binary value, and where p_i represents the propagate signal and is equivalent to a logical summation operation between a_i and b_i.

8. The parallel adder of claim 6, wherein the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals.

9. The parallel adder of claim 6, wherein the fourth logic stage implements an exclusive OR function to generate the summation signal.

11. The parallel adder of claim 6, wherein N is equal to 64.

12. The parallel adder of claim 6, wherein the logic stages are implemented with complementary metal oxide semiconductor components.

13. A method of adding, in parallel, a first *N*-bit binary value and a second *N*-bit binary value, the method comprising the steps of:

computing generate signals and propagate signals for each bit;

computing block generate signals and block propagate signals for groups of one through *m* bits from the generate and propagate signals computed in the first computing step;

combining the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

combining remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and generating a summation signal wherein the summation signal represents the dynamic logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation;

wherein the dynamic logical addition is performed without inversion of the generate signals, propagate signals, block generate signals and block propagate signals.

14. The method of claim 13, wherein a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i, wherein c_i is equivalent to $g_i + (p_i c_{i-1})$, where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i where a_i represents the first binary value and b_i represents the second binary value, and where p_i represents the propagate signal and is equivalent to a logical summation operation between a_i and b_i.

15. The method of claim 13, wherein the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals.

16. The method of claim 13, wherein the summation signal is generated in accordance with an exclusive OR function.

18. The method of claim 13, wherein N is equal to 64.

19. The method of claim 13, wherein the computing, combining and generating steps are implemented with complementary metal oxide semiconductor components.

20. A processing device having a dynamic N-bit parallel adder, the dynamic N-bit parallel adder comprising:

a first logic stage, the first logic stage configured to receive a first N-bit binary value and a second N-bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through m bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation;

wherein at least one of the logic stages has dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic.